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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/575,456	05/22/2000	James S. Cullum	M4065.0244/P244	2124

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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 08/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/575,456	CULLUM ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2003* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,10-16,18-20,24-30,32-34,38-47 and 49-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,10-16,18-20,24-30,32-34,38-47 and 49-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Amendment A and Drawing correction both dated 6/12/03.

2. Claims 1-2, 4-6, 10-16, 18-20, 24-30, 32-34, 38-47 and 49-51 are presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. The multiplexor as per claim 14 is not shown in any drawings. The fuse and anti-fuse element as per claim 41 (emphasis added) and dependent claims thereof are not shown in any drawings. Only fuse or anti-fuses are shown as described for figure 4. Therefore, the "at least one multiplexor" as per claim 14 must be shown or the feature(s) canceled from the claim(s). Therefore, the "fuse and anti-fuse" as per claim 41 and dependent claims thereof must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Applicant's arguments with respect to claims 1-2, 4-6, 10-16, 18-20, 24-30, 32-34, 38-47 and 49-51 have been considered but are moot in view of the new ground(s) of rejection.

6. Claims 1-2, 4-6, 10-13, 16, 18-20, 24-27, 29-34, 38-47 and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (hereinafter AAPA) in view of Ashuri U.S. Patent 5,652,530 (hereinafter Ashuri).

7. As to claim 1, AAPA substantially taught the invention as per claim 1 including:

a. a clock source for supplying a first clock signal [17 figure 1];

b. a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal [13a-13n figure 1];

AAPA does not expressly teach a plurality of adjustable delay circuits for receiving said first clock signal, each said of adjustable delay circuit providing a respective delay first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element for programming.

In summary, AAPA taught using a single delay for a clock for a plurality of output circuits wherein each output circuit has different data signal coupled to it input. The single delay of AAPA is not explicitly described in detail.

Ashuri, teaches a single output circuit having its own adjustable delay (delay shifter 310) providing a respective delayed first clock signal (from external clock 321) to an output circuit

(flip-flop 350), wherein each adjustable delay circuit contains a programming circuit (fuses 520 and capacitors 530) for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element (fuse elements 520) for programming [figures 3 and 5 and corresponding text]. In summary, Ashuri teaches an apparatus having a particular data signal for an output circuit that also has an associated adjustable delay. The invention of Ashuri ensures that a clock signal is delayed by an appropriate amount relative to a delay with associated data signal.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA by removing the single delay of AAPA and placing a delay as taught by Ashuri for each output circuit into the respective clock line because both AAPA and Ashuri are directed toward placing data into a clock signal. This modification results in the applicants claimed invention. That is, each output circuit has it own associated adjustable delay circuit. An artisan would have made the modification because Ashuri teaches that in his invention that a clock signal will (and should) be delayed by an appropriate amount for each data signal. Ashuri further teaches that the adjustable delay for the clock is desirable because it allows the data signal to be sampled at an appropriate time and that the delay is adjustable to accommodate different amounts of propagation delay for a particular data signal [col. 1 lines 21-60].

8. As to claim 2, AAPA combined with Ashuri taught the data output apparatus according to claim 1, described above. Ashuri further taught wherein each of the output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit [figure 3 col. 3 lines 13-23]. Ashuri teaches that the delay added should correspond to the delay in the particular data line.

9. As to claim 4, AAPA combined with Ashuri taught the data output apparatus according to claim 2, described above. AAPA together with Ashuri do not expressly disclose wherein the delay of each of said adjustable delay circuits is adjusted such that time of said data hold time of each of said output circuits is substantially coincident. However, because the delay as taught by Ashuri is now implemented in each clock path wherein each of the adjustable delay circuits is adjusted accordingly. Each output circuit signal path length differences and other timing aberrations caused by the circuit topology within the chip, as described by AAPA, are now compensated by the modification with Ashuri. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the data hold time of each output circuit substantially coincident because doing so would allow the plurality of data signal to be aligned, which is desirable in AAPA to reduce the time to output the data to a device.

10. As to claim 5, AAPA combined with Ashuri taught the data output apparatus according to claim 2, described above. As to claim 5, AAPA teaches that the output circuits would be connected to data output terminals because the output circuit are used to place output to a memory device thus requiring output terminals [page 2 lines 1-2]. AAPA together with Ashuri do not expressly disclose wherein the delay of each of said adjustable delay circuits is adjusted such that time of said data hold time of each of said output circuits is substantially coincident. However, because the delay as taught by Ashuri is now implemented in each clock path wherein each of the adjustable delay circuits is adjusted accordingly. Each output circuit signal path length differences and other timing aberrations caused by the circuit topology within the chip, as described by AAPA, are now compensated by the modification with Ashuri. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the data

hold time of each output circuit is now substantially coincident because doing so would allow the plurality of data signal to be aligned, which is desirable in AAPA to reduce the time to output the data to a device.

11. As to claim 6, AAPA together with Ashuri taught the data output apparatus according to claim 1, described above. AAPA combined with Ashuri further wherein each of said delay element comprises:

a. an input (input to delay shifter 510) for receiving said first clock signal [Ashuri – figure 5];

b. a plurality of delay elements (capacitors 530), each of said delay elements providing different respective delay to a signal applied thereto [Ashuri - figure 5 and corresponding text]; and

c. a switch circuit (control lines for selecting fuses 520) for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to respective output circuit [Ashuri - figure 5 and corresponding text].

12. As to claim 10, AAPA together with Ashuri taught the data output apparatus according to claim 6, described above. Ashuri further taught wherein said switch circuit comprises a plurality of switch elements (selecting control lines to select fuses 520) respectively coupled to said plurality of delay elements (capacitors 530), one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element [figure 5 and related text].

13. As to claim 11, AAPA together with Ashuri taught the data output apparatus according to claim 10, described above. Ashuri further taught comprising a programmable circuit for

programming which of said switch elements (control lines are selected to enable/disable the fuses) is selectively enabled [col. 3 lines 47-53]. Ashuri suggests that a programmable circuit is user to selective enable switch elements by disclosing that that control lines may be used to allow a user to select fuses.

14. As to claim 12, AAPA together with Ashuri taught the data output apparatus according to claim 1, described above. AAPA further taught wherein the output circuits are output buffer circuits [AAPA - figure 1].

15. As to claim 13, AAPA together with Ashuri taught the data output apparatus according to claim 1, described above. AAPA further taught wherein each of said output circuits receives and outputs a respective data signal from a memory array [figure 1 and pages 1 line 11 through page 3 line 2].

16. As to claims 15-16, 18-20, 24-27, 29-30, 32-34 and 38-40, AAPA together with Ashuri taught the claimed data output apparatus therefore they also teach the claimed processor based system and the claimed memory device.

17. As to claim 41, AAPA taught a method of providing data output signal comprising:

a. receiving a plurality of data output signals at respective output circuits [figure 1];

b. operating said output circuits in response to respective applied clock signals to make data output signals available at the output of said output circuits [pages 1 line 11 through page 3 line 2].

c. providing a first clock signal [clock 17, figure 1];

AAPA does not expressly teach generating each said respective applied clock signal from said first clock signal, each respective applied clock signal having a respective adjustable delay relative to said first clock signal.

In summary, AAPA taught using a single delay for a clock for a plurality of output circuits wherein each output circuit has different data signal coupled to it input. The single delay of AAPA is not explicitly described in detail.

Ashuri, teaches a single output circuit having its own respective adjustable delay (delay shifter 310) providing a respective delayed first clock signal (from external clock 321) to an output circuit (flip-flop 350), wherein each adjustable delay circuit contains a programming circuit (fuses 520 and capacitors 530) for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element (fuse elements 520) for programming [figures 3 and 5 and corresponding text]. In summary, Ashuri teaches an apparatus having a particular data signal for an output circuit that also has an associated adjustable delay. The invention of Ashuri ensures that a clock signal is delayed by an appropriate amount relative to a delay with associated data signal. Ashuri further implicitly teaches that anti-fuses would be applicable to his invention because in using fuses one of ordinary skill would have readily recognized that anti-fuses would be just as effective in selecting the delay amount either in combination with fuses or in substitution of fuses. Therefore, using fuses and/or anti-fuses does not depart from the scope of Ashuri's invention.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA by removing the single delay of AAPA and placing a delay as taught by Ashuri for each output circuit into the respective clock line because both AAPA and Ashuri are directed

toward placing data into a clock signal. This modification results in the applicants claimed invention. That is, each output circuit has it own associated adjustable delay circuit. An artisan would have made the modification because Ashuri teaches that in his invention that a clock signal will (and should) be delayed by an appropriate amount for each data signal. Ashuri further teaches that the adjustable delay for the clock is desirable because it allows the data signal to be sampled at an appropriate time and that the delay is adjustable to accommodate different amounts of propagation delay for a particular data signal [col. 1 lines 21-60].

18. As to claims 42-47 and 49-51, they are rejected on the same basis as set forth hereinabove.

19. Claims 14 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Ashuri as applied to claim 6 above and in further view of Heuring and Jordan, "Computer Systems and Architecture" (hereinafter Heuring).

20. As to claim 14, AAPA together with Ashuri taught the data output apparatus according to claim 6, described above. AAPA together with Ashuri do not expressly disclose wherein said switch circuit comprises at least one multiplexor. Ashuri discloses using a set of control lines to allow a user to select individual fuses [col. 3 lines 49-53].

Heuring taught using muliplexor ("multiplexer") to output a particular value (either a 1 or 0 to perform a function) given a set of control lines (A and B) [pages 497-499]. Heuring teaches that multiplexors are used to implement Boolean functions.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA and Ashuri by implementing the selection of the fuses by using a multiplexors

as taught by Heuring because both use control lines to perform a Boolean function (selecting fuses). An artisan would have been motivated to use multiplexors because Heuring teaches that multiplexor are widely used because there generality simplifies the design process and there modularity simplifies the implementation [page 498 last sentence of first paragraph].

21. As to claim 28, AAPA together with Ashuri and Heuring taught the claimed data output apparatus therefore together they also teach the claimed processor-based system.

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

> U.S. Pat. No. 4,903,223 to Norman et al. This patent teaches that fuses and anti-fuses may be used interchangeably as programming elements.
>
> European Pat. No. EP 213641 A2 to Sakata et al. This patent teaches using delay elements in a transmitter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

James Trujillo
August 18, 2003

THOMAS LEE
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